TARGET OPERATIVE MODE

In EICASLAB**,** the ***Target operative mode*** enables the designer to perform the following activities:

- **to generate the code for the hardware target**, the Basic Software (BS) necessary to run in the final Hardware Target the same Application Software (AS) already tested in the previous operative modes (Modelling & Like Real-time Simulation and Rapid Control Prototyping);

- **to generate the HIL Manager tool and the TARGET Manager tool for the RCP Platform,** that allows to test in real-time the target code in two different modalities: Hardware-In-the-Loop and Final Validation Test. The EICASLAB RCP Platform is suitably connected to the final Hardware Targets and provides the necessary features to support at best both the activities.

The Target mode is provided by the following software modules, available as add-on of the SIMBUILDER tool: the **ACGAS module**, the **RCP module,** the **TARGET module** and the **HIL/FVT module**.

ACG IN TARGET OPERATIVE MODE

The Automatic Code Generation (ACG) is the EICASLAB feature that assists the control designer in generating the code corresponding to the designed control strategy, for performing the testing activities foreseen in each operative mode.
In Target mode, EICASLAB automatically generates special real-time software code (AS + BS) for the RCP Platform and the Hardware Target(s), in order to perform the Hardware-in-The-Loop and the Final Validation Test.

In addition to the **ACG for Application Software** and the **ACG for Rapid Control Prototyping** the TARGET operative mode requires the following ACG components:

- **ACG for Hardware Target**, that generates the code for the final target (*Target* phase);

- **ACG for HIL**, that generates the HIL Manager tool for performing the Hardware-In-the-Loop activity (*Target* phase).

- **ACG for FVT**, that generates the TARGET Manager tool for performing the Final Validation Test activity (*Target* phase).

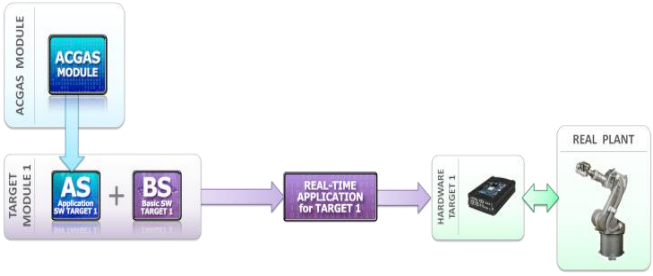
TARGET Highlights

- **Enable Hardware-In-the-Loop process and final validation test in EICASLAB**
- **Powerful multi-threading and multi-core programming techniques**
- **Automatic code generation for different HW target families**
- **Easy configuration of HW interfaces and control activities real-time scheduling**
- **EICASLAB RCP Platform used for host & supervisor PC, data monitoring and data recording**

Control Tuning

ACG for Hardware Target

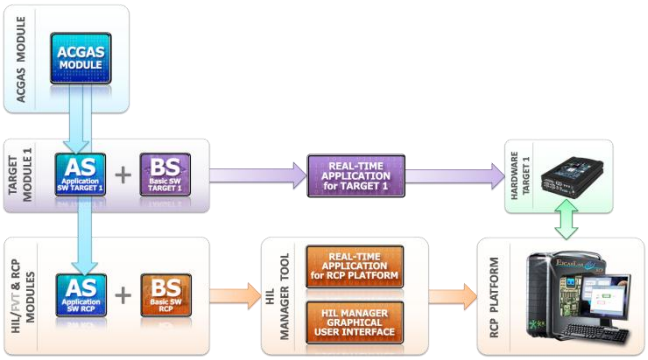
The *ACG for HW Target* is the EICASLAB feature aiming at generating the target-dependent source code for a set of pre-selected targets.
Required modules: ACGAS , TARGET.



ACG for Hardware Target

ACG for Hardware-In-the-Loop

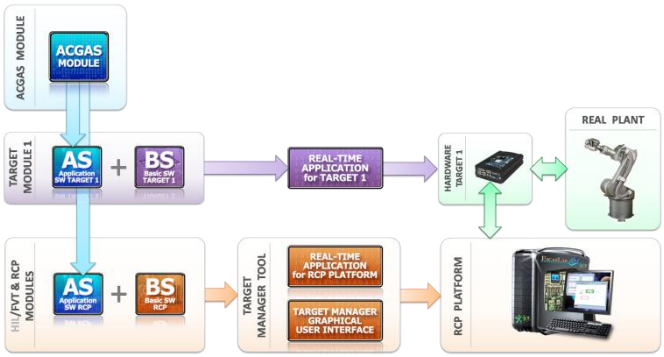
The *ACG for HIL* is the EICASLAB feature aiming at generating the BS necessary for performing the Hardware-In-the-Loop activities through the HIL Manager tool.
Required modules: ACGAS , RCP, TARGET, HIL/FVT.



ACG for HIL

ACG for Final Validation Test

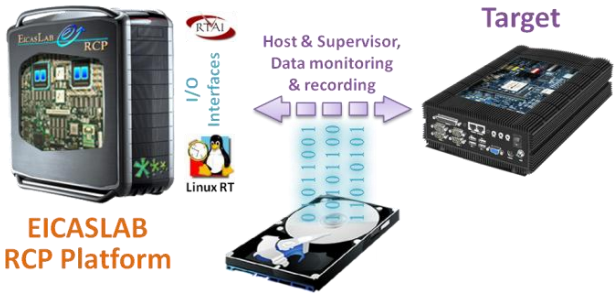
The *ACG for FVT* is the EICASLAB feature aiming at generating the BS necessary for performing the Final Validation Test activities through the TARGET Manager tool.
Required modules: ACGAS , RCP, TARGET, HIL/FVT.



ACG for FVT

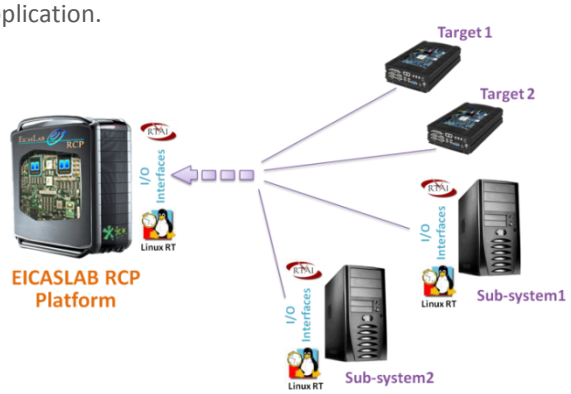
HARDWARE IN THE LOOP (HIL) SUB-MODE & HIL MANAGER

In ***Hardware-In-the-Loop*** (HIL), the control application works in real-time the Hardware Target, whereas the real plant is simulated in real-time in the RCP Platform. In the related testing scenario, the RCP Platform is connected to the Hardware Target module(s) to work also as host computer/supervisor, by providing full control on the HIL trials, data recording and system monitoring capabilities.

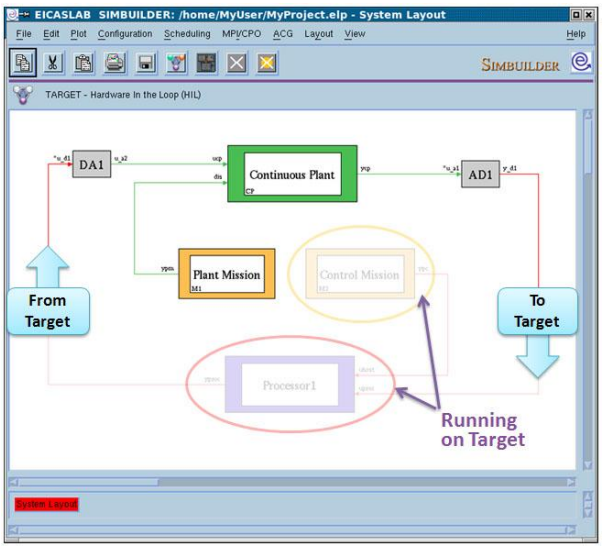


Hardware-In-the-Loop scenario

The ***Hardware-In-the-Loop*** is the EICASLAB operative mode that allows you to predispose whatever testing scenario can be useful for testing and validating your application.



When the ***Hardware-In-the-Loop*** sub-mode is enabled, the System Layout of SIMBUILDER provides – as a default – the following scenario (refer to the previous HIL figure):

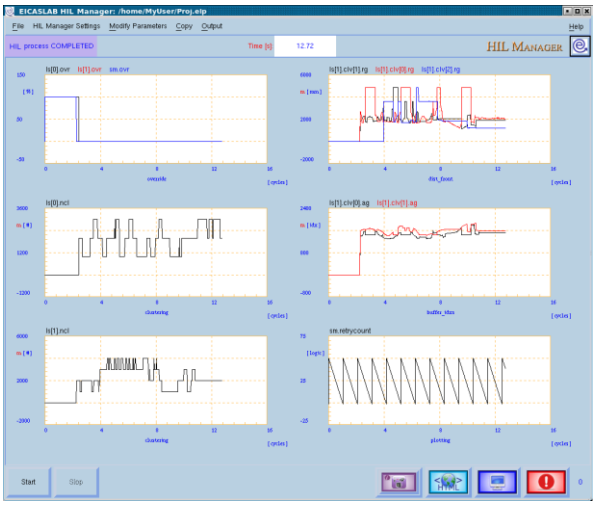


Default HIL System Layout

SIMBUILDER automatically generates the real-time code for HIL by means of the installed software modules, according to the enabled/disabled blocks and the ACG settings provided in the System Layout.

The **HIL Manager tool**, generated by the **HIL/FVT module**, is executed in real-time in the EICASLAB RCP Platform, that provides a suitable RTOS (Linux RT or Linux RTAI with pre-emption patch) for running the real-time code and the suitable input/output interfaces, necessary to exchange data and/or commands with the Hardware Target(s).

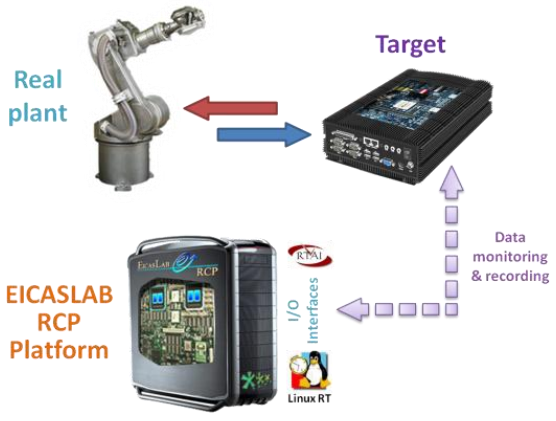
The **HIL Manager tool** allows to manage the overall ***Hardware-In-the-Loop*** process, to verify in real-time the control performance thanks to the direct feedback provided by the Target Manager GUI and to record the trial results for further post-processing analysis.



HIL Manager GUI

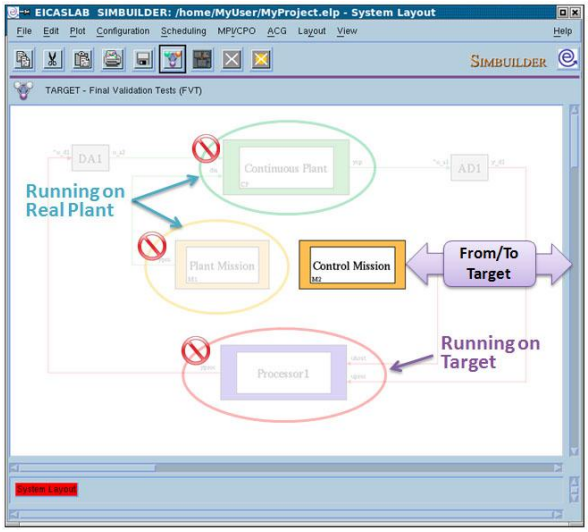
THE FINAL VALIDATION TEST SUB-MODE & TARGET MANAGER

When the ***Final Validation Test*** (FVT) is enabled, the control application works in real-time in the Hardware Target, which is directly connected to the real plant. If needed, the RCP Platform can be connected to the target to work as host computer/supervisor, by providing trial management, data recording and system monitoring capabilities, as well as to operate as control mission.



Final Validation Test scenario

The System Layout of SIMBUILDER provides – as a default – the following scenario (see the previous HIL figure):

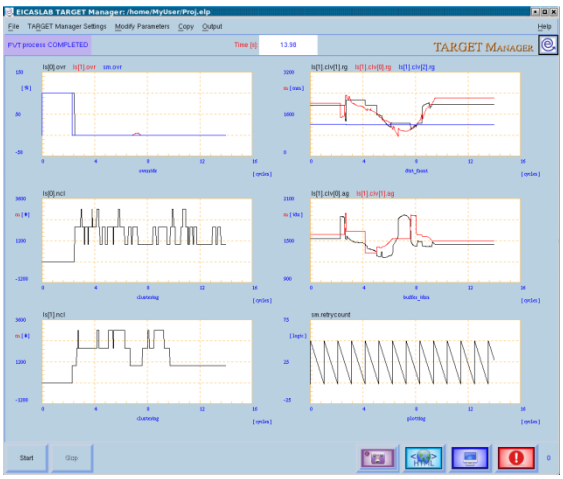


Default FVT System Layout

According to the enabled/disabled blocks and the ACG settings, SIMBUILDER automatically generates the real-time code by means of the dedicated software modules, already mentioned above.

The **Target Manager tool**, generated by the **HIL/FVT module**, is executed in real-time in the EICASLAB RCP Platform, that provides a suitable RTOS (Linux RT or Linux RTAI with pre-emption patch) for running the real-time code and the suitable input/output interfaces, necessary to exchange data and/or commands with the Hardware Target(s).

The **Target Manager tool** allows to manage the overall ***Final Validation Test*** process, to verify in real-time the control performance thanks to the direct feedback provided by the Target Manager GUI and to record the trial results for further post-processing analysis.



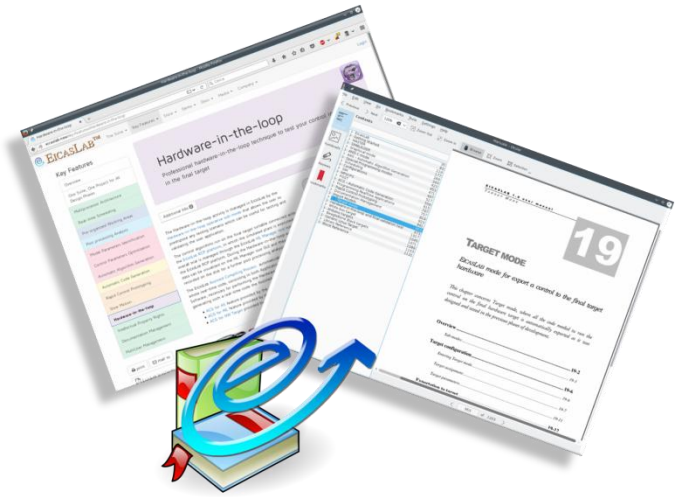
TARGET Manager GUI

MANUAL & DOCUMENTATION

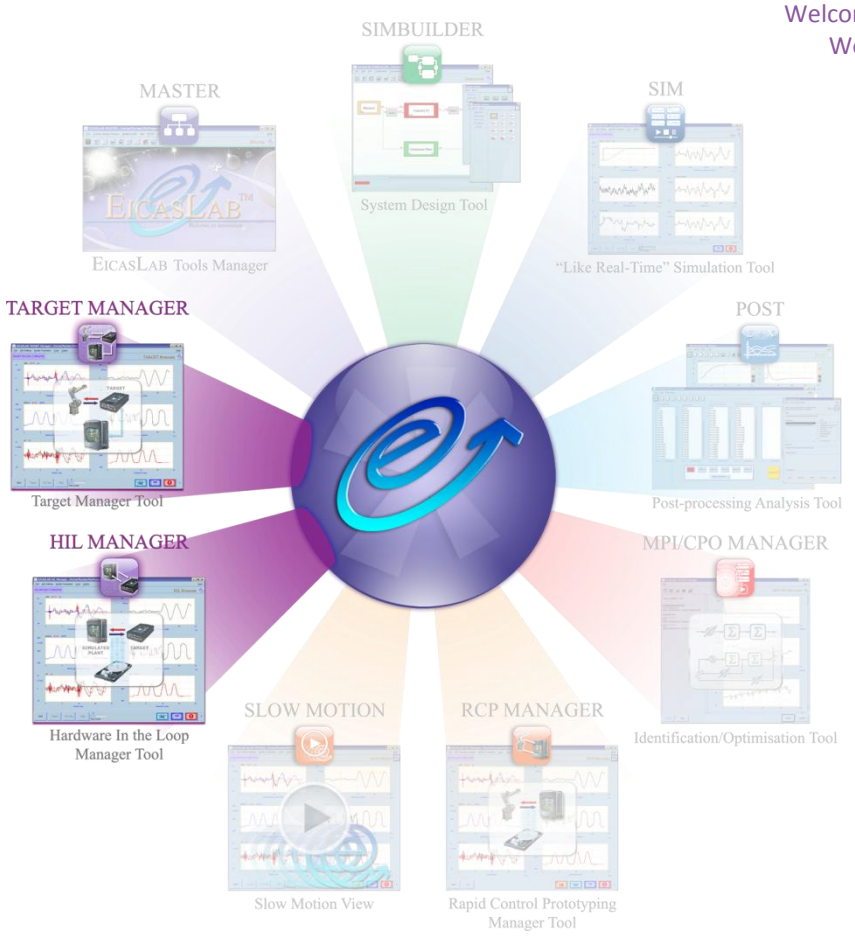
The EICASLAB TARGET mode provides the user with all the necessary support for performing at best the Hardware-In-the-Loop activities and the final validation test:

- a specific chapter of the EICASLAB User Manual is devoted to illustrate the overall TARGET mode capabilities for helping the user to make profit in using the EICASLAB software;
- the EICASLAB website can be directly accessed to get information, to contact us, to buy new EICASLAB software modules and extend the capabilities of your professional control design suite.

Our service support is always at disposal of our Customers with the aim to guarantee the best assistance.



Welcome to EICASLAB Suite.
Welcome to Innovation!



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